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(54) Title of invention INSULATED GATE TRANSISTOR

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SPECIFICATION

1. TITLE OF INVENTION

INSULATED GATE TRANSISTOR

2. SCOPE OF PATENT CLAIMS

(1) Insulated gate transistor wherein, on a primary surface of a semiconductor substrate of a first conductivity type, first and second regions of a second conductivity type are formed with a required gap maintained between, with an insulation film formed over the area where the channel between the said first and second regions is to be formed, and a gate electrode is formed over this gate insulation film, said transistor being distinguished in that it comprises, in said first or second region of the second conductivity type, a region of the first conductivity type which, in the widthwise direction channel, is sandwiched depthwise by said first or second region and has a region of said second conductivity type at the surface side, so as to be wrapped in said first or second region in the lengthwise direction of the channel, and which is electrically connected to said semiconductor substrate.

(2) An insulated gate transistor as set forth in Claim 1, distinguished in that it comprises a first or second region of said second conductivity type; a third or fourth region with a lower concentration of dopants than said first or second region of the second conductivity type, introduced from the surface in the region of the first conductivity type where the channel in this first or second region is to be formed; and, in said third or fourth region, a region of the first conductivity type with a higher dopant concentration than said semiconductor substrate, which, in the widthwise direction of the channel, is sandwiched depthwise by said third or fourth region and has a region of said second conductivity type at the surface side so as to be wrapped in said first and third or second and fourth regions in the lengthwise direction of the channel, and which is electrically connected to said semiconductor substrate.

(3) An insulated gate transistor as set forth in Claim 2, distinguished in that it comprises a gate electrode region up to the top of the region of the first conductivity type formed so as to be wrapped in the first or second region of the second conductivity type in the lengthwise direction of the channel.

3. DETAILED DESCRIPTION OF THE INVENTION

(*Objective of the invention*)

(*Field of industrial application*)

This invention relates to the structure of insulated gate field effect semiconductor devices.

(*Prior art*)

Currently, progress is being made in micronization of elements in order to improve the operating characteristics and increase the integration of semiconductor devices using insulated gate field effect transistors (hereinafter, MISFET), but if micronization is increased while keeping the same supply voltage, high electric field regions will appear within the element, generating hot carriers and causing problems in terms of reliability. To deal with this problem, for example the LDD (Lightly Doped Drain) structure has been proposed, whereby low concentration regions (404) and (404′) are provided in the source (402) or drain (403) area of a MISFET, as shown in Figure 4, to reduce the electric field. Here, (405), (405′) and (406) are respectively the drain, source and gate electrode, (407) is the gate insulation film, and (408) is the insulation protective film. However, there is the problem that, unless the concentration of this low concentration region is at or above a certain level, the trap charge in the gate will cause gm to deteriorate, so it cannot be lowered without limit. In this connection, a structure has been proposed as shown in Figure 5, where a high concentration doping region (409) of the same conductivity type as the substrate is provided over the surface in the low concentration drain region (IE^3 Trans. ED–33 No. 11 P. 1769 (1986), S. BAMPI and J. D. PLUMMER). With this structure, as shown in Figure 6, a JFET is connected in series to the MISFET. Here, the V_S, V_Q, V_P and V_{SUB} in Figure 5 and Figure 6 correspond to each other. Therefore, the voltage between the source and drain is split between the MISFET and JFET, so even if one increases micronization at a given supply voltage, no high electric field region will form on the MISFET side. Moreover, with this structure, even in regions with relatively high electric fields, the position where current flows is deeper down from the surface compared to MISFETs of conventional structure and LDD structure, so this is a structure that can control the problem of reduced reliability due to hot carriers. However, with regard to the drain current/voltage characteristics, there has been the problem that, as shown in Figure 7, for instance at 3V or lower, the current drive capacity is lower, and switching operations become slower.

(*Problem to be solved by the invention*)

As discussed above, in the aforementioned improved LDD MISFETs, there has been the problem that current drive capacity drops where drain voltage is low, and switching operations become slower. The objective of the present invention is to provide a transistor whereby all impressed drain voltage will go toward MISFET drive voltage and the JFET will turn on when the drain voltage is high, thereby effectively reducing the voltage applied to the MISFET and resolving the aforementioned problems, which will have no reliability problems and will operate with good characteristics even when micronized.

(*Constitution of the invention*)

(*Means of solving the problem*)

To achieve the aforementioned objective, the present invention is distinguished in that a high concentration region of the same conductivity type as the substrate formed in the low concentration drain region is formed away from the surface, the gate electrode is formed above that, and a channel forms on the surface and current flows there when the drain voltage is low.

(*Function*)

In the present invention, a high concentration region of the same conductivity type as the substrate formed in the low concentration drain region is created at a location below the surface, and the gate electrode is formed above that; thus, when adequate voltage for a MISFET channel to be formed is impressed onto the gate electrode and drain voltage is increased, the current first flows along the surface to reach the drain, and as drain voltage is increased further, a depletion layer extends around the high concentration region, and current starts to flow at a deeper position, preventing hot carriers from being injected into the gate oxidation film, thus implementing a transistor whereby reliability will not drop and high speed operation performance will not be harmed even if micronization is increased.

(*Embodiments*)

Figure 1 is a cross-sectional view in the lengthwise direction of the channel of an improved n channel LDD MOSFET illustrating an embodiment of the present invention. A cross-section along line A–A′ in the widthwise direction of the channel in this drawing is shown in Figure 2. As can be seen in Figure 2, the p^+ region 105 is given V_{SUB} impressed onto the substrate 101 through the p^+ region 205 which forms the channel stopper beneath the field oxidation film 209. As one applies a voltage V_a adequate for reversal of the MOSFET channel area to n^+ polySI gate electrode 106 and continues increasing the drain voltage V_D, the

channel comes to encompass the n^- low concentration drain region 104', and the current flows through the surface from the source 102 to the drain 103. As drain voltage is raised further, the depletion layer widens at the juncture of the p^+ region 105 and the n^- regions 104 and 104', and the current path gradually moves deeper down (below the p^+ region 105) away from the surface (above the p^+ region 105). Therefore, even when the drain voltage V_D is sufficiently high and hot carriers would form due to high electric fields in the vicinity of the surface with conventional structures and LDD structures, with the structure as per the present invention, the generation of hot carriers occurs in a deep area away from the gate oxidation film, so it does not reduce reliability. Furthermore, when the drain voltage V_D is not so high as to cause problems of hot carrier generation, the current flows along the surface, allowing devices to be obtained with the same current drive capacity as conventional LDD structures.

In Figure 3 (a) through (e), a manufacturing method for the n channel MOSFET as per the embodiment of the present invention shown in Figure 1 is illustrated by means of a cross-sectional drawing in the lengthwise direction of the channel. First, using conventional n channel MOSFET structure technology, an element separation field oxidation film 302 and a gate oxidation film 303 are formed over the p^- substrate 301, and a gate electrode 304 is created over said gate oxidation film 303 (Figure 3 (a)).

Next, a resist 305 is formed over a portion of the substrate 301 and phosphorus (P) is ion injected into the area not covered by the resist 305, after which an n^- region 306 is created as the drain area by thermal diffusion (Figure 3 (b)).

Next, BF_2 is ion injected, forming a p^+ region 306a in said n^- region 306 (Figure 1 (c)).

Furthermore, As is ion injected, making the surface part of said p^+ region into an n^- region (Figure 1 (d)).

Subsequently, said resist is removed, poly Si is deposited, and said polySi 308 is left on the side walls of said gate electrode 304 and made to overlap the p^+ region 307 as a part of the gate electrode. Next, using this as a mask, the source and drain regions 310 and 309 are formed by As ion injection at least to the depth of the area between said p^+ region 306a and n^- region 306.

Thereafter, an insulation film is deposited over the entire surface, opening contact holes connecting to the source and drain regions in this insulation film and forming electrodes in the source and drain areas to complete the transistor of the structure shown in Figure 1. While in the present embodiment, the structure of the present invention was applied only to the drain part, there is no problem with applying the structure of the present invention also to the source part; the structure of the present invention can also be applied in places where current needs to flow bidirectionally.

(*Effect of the invention*)

According the present invention as described above, a transistor can be implemented which allows decreased reliability due to the hot carrier effect to be controlled and which has high speed operation performance even if micronization is increased while keeping the supply voltage constant.

4. BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a cross-sectional view in the lengthwise direction of the channel of an improved n channel LDD MOSFET as per one embodiment of the present invention; Figure 2 is a cross-sectional view in the widthwise direction of the channel along A–A' shown in Figure 1; Figure 3 is a cross-sectional view illustrating the manufacturing process for the improved n channel LDD MOSFET show in Figure 1; Figure 4 is a cross-sectional view in the lengthwise direction of the channel of a conventional LDD structure MOSFET; Figure 5 is conventional improved structure provided with a p^+ region over the surface in the drain n^- region of an n channel LDD MOSFET; Figure 6 is a drawing which represents the structure of Figure 5 as an equivalent circuit; Figure 7 shows the drain voltage/drain current characteristics of the structure of Figure 5 in comparison to the conventional structure.

101, 301, 401 ··· p type semiconductor substrate;
102, 103, 309, 310, 402, 403 ··· high concentration n type diffusion region;
104, 104', 306, 404, 404' ··· low concentration n type diffusion region;
105, 205, 307 ··· high concentration p type diffusion region;
106, 304, 308, 406 ··· gate electrode;
107, 303, 407 ··· gate insulation film;
108, 408 ··· insulation protective film;
209, 302 ··· field insulation film.

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[see source for figures]

Figure 1

Figure 2

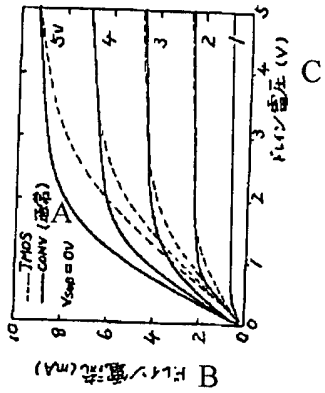
Figure 3

Figure 4

Figure 5

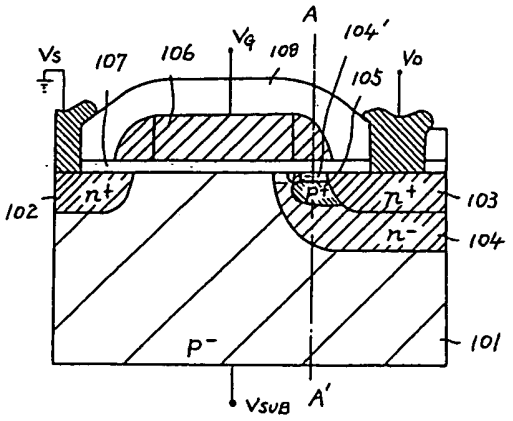
Figure 6

Figure 7

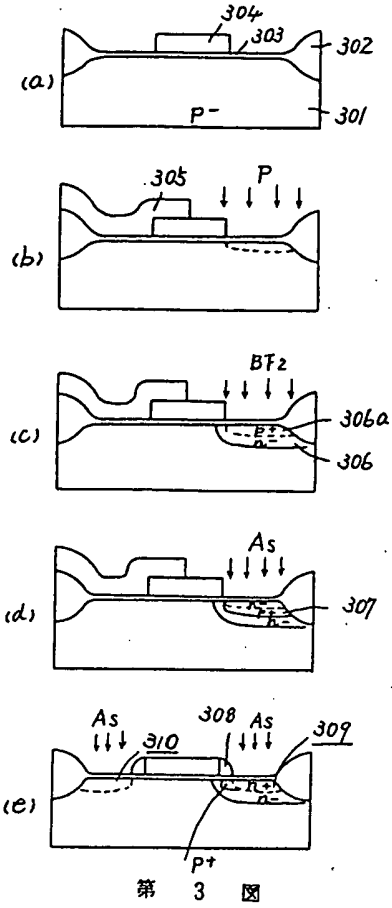


[keys]

A: Conventional
B: Drain current (mA)
C: Drain voltage (V)



第 1 図



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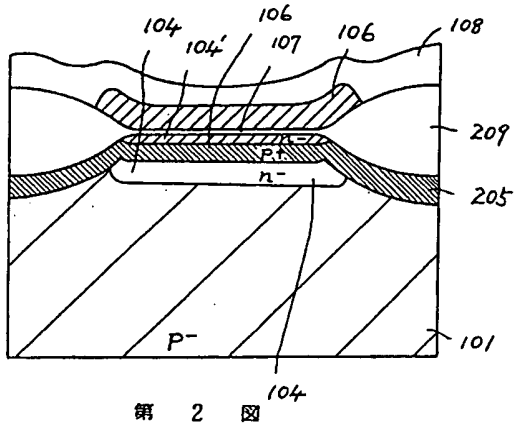
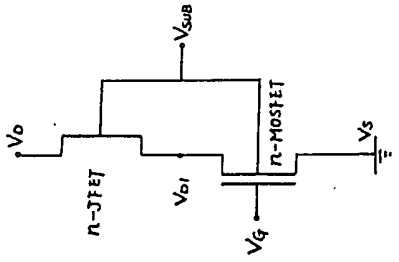


第 2 図



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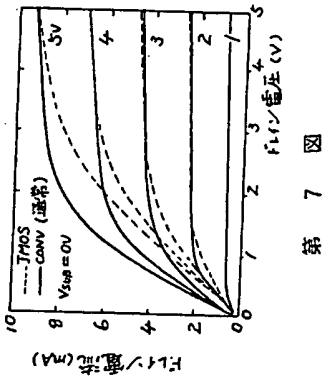
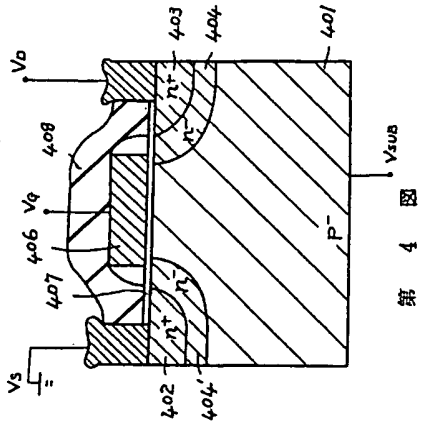
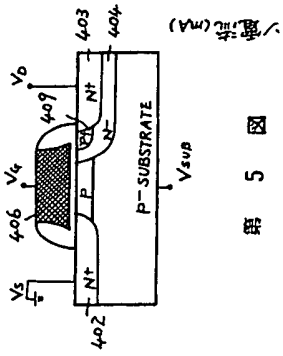


第 7 図



第 4 図



第 5 図